

were rejected. These claims were rejected either under 35 U.S.C. 102(e) as being anticipated by Bobry, U.S. Patent No. 5,593,236, or under 35 U.S.C. 103(a) over Bobry in view of one of several additional references as noted below. Claims 2 and 13-16 have been cancelled. Claim 17 has been rewritten in independent form and claims 18 and 19 have been amended to change their dependence from now cancelled claim 13 to claim 17. The Applicants thank the Examiner for the amendment to claim 29.

For the reasons stated below, all of the pending claims are believed to be allowable. These Remarks will discuss the various claims grouped according to their numerical order, although this differs somewhat from the order in which they occur in the Office Action.

Claims 4-9, 11-12, 17-19, and 20-24

Claims 4-6 and 8-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Bobry. Concerning claim 4, this recites in its last element "an activation circuit that activates the functional unit in response to the input signal from the speaker ... and begins an output operation to drive the speaker in response to being activated by the activation circuit." It is respectfully submitted that this feature is absent in Bobry. The relevant portion of Bobry cited in the Office Action (column 14, lines 57-64) states:

Further, with appropriate voice recognition software, the apparatus 10 can be made responsive to voice commands. For example, the spoken phrase 'print confidential' would cause the device to retrieve the word CONFIDENTIAL from its memory and set itself to print that word. Similarly, voice synthesis software could be used to provide spoken communications from the printer to the user, such as, for example, 'ink supply is low.'

This describes two separate processes, namely printing in response to a voice command and a synthesized spoken communication from a part of the device. It does not describe "an output operation to drive the speaker" due to "the input signal from the speaker". It is respectfully submitted that the device of claim 4 is not presented in Bobry and that the rejection under 35 U.S.C. 102(e) is not well founded and that claim 4, along with dependent claims 5-7, are allowable.

Claim 8 is also rejected, and claim 5 further rejected, under 35 U.S.C. 102(e) as being anticipated by Bobry. In addition to the other elements, both of these claims contain "a memory array" on the same integrated circuit as the other elements. Bobry does show memory 46 in its Figure 14A. There is, however, no description of a memory array on the same circuit as the other elements. Consequently, it is respectfully submitted that the system

of claims 5 and 8 are not presented in Bobry and that the rejection under 35 U.S.C. 102(e) is not well founded and that claims 5 and 8, along with dependent claims 6 and 9, are allowable (or further allowable).

With respect to the obviousness rejection of claims 11 and 12 under 35 U.S.C. 103(a), the cited Dallas Semiconductor data sheet does show a three-pin integrated circuit. Further, it does state “[a]pplications include portable computers, portable/cellular phones, and handheld instrumentation.” However, as the rest of the Dallas Semiconductor data sheet makes clear, this is for the *battery pack of these devices*, and in particular for providing an ID number for the battery pack: It does not suggest placing the portable computers and other devices themselves into such a package. It is respectfully submitted that the Office Action has misinterpreted the Dallas Semiconductor data sheet and that it is far from obvious to combine all of the elements found in claim 11 into such a 3-pin package. Thus, the rejection of claims 11 and 12 under 35 U.S.C. 103(a) is believed to be in error and that these claims are allowable.

The Office Action has rejected claim 17 under 35 U.S.C. 103(a) as being unpatentable over Bobry in view of Giles et al. Claim 17 has been rewritten in independent form by incorporating the elements of claims 13-16. Claims 18 and 19 have been amended to change their dependence from now cancelled claim 13 to claim 17. Claim 17 presents a single integrated circuit comprising a large number of elements, including a “a memory array; a read circuit...reading from the memory array a series of values representing a sound; and a write circuit...writing to the memory array a series of values representing the input signal.” Bobry does present memory (46 of Figure 14A); however, neither of the references present both read and write circuit to respectively read from the array “a series of values representing a sound” and write to the array “a series of values representing the input signal.” Further, it is not believed obvious in light of these references to place all of these elements on a single integrated circuit. Bobry only states (column 14, lines 46-48) that “[s]ome microprocessors contain such [A/D and D/A] converters as an integral part, in which case separate devices are not needed”, but beyond this the references neither teach nor suggest combining the dispirit elements of claim 17 on a single integrated circuit. This believed to be non-obvious and, consequently, claims 17-19 are believed allowable, with claim 19 further believed allowable for the reasons discussed with respect to claim 11.

Claims 20 and 21 are also rejected upon 35 U.S.C. 102(e) as being anticipated by Bobry for the same reasons cited with respect to claim 4. As in the above discussion of

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claim 4, this rejection under 35 U.S.C. 102(e) is not believed to be well founded. In particular, the teachings of Bobry do not describe “in response to activating the functional unit, generating an output signal from the functional unit through the terminal to the speaker, wherein the output signal drives the speaker to produce a sound.” Therefore, claim 20 and its dependent claims, claims 21-24, are believed allowable.

Claims 25-28

Claims 25-28 each contain a limitation not found in their base respective underlying claims. These are rejected by the Office Action under 35 U.S.C. 102(e) with the statement “The limitations of these claims are anticipated by Bobry as shown above.” In fact, the referred to preceding comments are largely those made in the previous Office Actions before these claims were added so that the limitations of these claims are nowhere discussed in the Office Action, either “as shown above” or elsewhere. Furthermore, the limitations of these claims are not found in Bobry. In addition to being believed allowable due to their base claims (respectively claims 6, 9, 17, and 20), these claims are further believed allowable based on these additional limitations.

Claims 25-28 are drawn to the particular embodiment where the sound output has been previously recorded in the memory array by use of the speaker. This ability to use the speaker as an input to record sound in the memory array of the integrated circuit that can then be played back through this same speaker when activated, again through the use of this speaker, is described, for example, in the Summary of the present application on page 3, lines 10-21: “The movement of the speaker diaphragm generates an input signal that activates the system function, for example, by activating playback of a previously recorded signal.” Such a process is not found in Bobry and it is respectfully submitted that a rejection of these claims under 35 U.S.C. 102(e) is without foundation and should be withdrawn.

Claims 29-36

As with claims 25-28, new claims 29-36 are also drawn a circuit and method where sound may be recorded and played back through the same input/output pin in response to a single also supplied through this input output pin. This is again a process neither described nor suggested in Bobry or the other cited references.

The use of a single integrated circuit possessing both a memory array and sound processing circuitry, allowing a single pin to both provide an audio signal to write into

the array and output a representation of this audio signal from the array, contains a number of elements not found in nor believed obvious based on the cited prior art. As discussed above with respect to claim 17, the cited prior art does not include the array, sound processing circuit, write circuit, and read circuit in a single integrated circuit. As discussed above with respect to claims 25-28, the references also do not include the ability to use the pin as an input to record sound in the memory array of the integrated circuit which can then be played back through this same pin. For any of these reasons claims 29-36 are believed allowable.

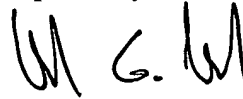
Conclusion

For any of these reasons, reconsideration of the Office Action's rejection of claims 4-9, 11, 12, and 17-36 is therefore respectfully requested, and an early indication of their allowability is earnestly solicited.

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Respectfully submitted,



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Appendix

Marked-Up Versions of Amended Claims

17.(Twice Amended) [The]An integrated circuit [of claim 16,] comprising:
an input/output pin;
a sound processing circuit;
an output circuit coupled to the input/output pin, wherein the output circuit
applies to the input/output pin an output signal representing a sound;
an activation circuit coupled to the input/output pin and the functional unit,
wherein in response to an input signal from the input/output pin, the activation circuit
activates the sound processing circuit;
an input circuit coupled to the input/output pin, wherein the input circuit, when
active, transfers the input signal received from the input/output pin to the sound processing
circuit; and
a control circuit coupled to the sound processing circuit, wherein the control
circuit selects an operation performed by the processing circuit when the activation circuit
activates the sound processing circuit, and
wherein the sound processing circuit comprises:
a first functional unit that performs an output operation to generate a
signal to the output circuit and a second functional unit that performs an input
operation to processes the input signal from the input circuit;
a memory array;
a read circuit coupled to the memory array, wherein the read circuit is
part of the first functional unit and the output operation includes reading from the
memory array a series of values representing a sound; and
a write circuit coupled to the memory array, wherein the write circuit is
part of the second functional unit and the input operation includes writing to the
memory array a series of values representing the input signal.

18.(Twice Amended) The integrated circuit of claim 17[13], wherein the
activation circuit comprises a delay element coupled to prevent the activation circuit from
activating the sound processing circuit during a delay period following completion of an
operation by the sound processing circuit.

19. (Amended) The integrated circuit of claim 17[13], further comprising a die and a three-pin package in which the die is mounted, the three-pin package having exactly three pins including the input/output, a pin for connection to a power supply, and a pin for connection to ground.

Pending Claims

(Claims 1-3 have been cancelled.)

4.(Amended) A sound processing system comprising:
a speaker;

an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:

an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an output signal to drive the speaker;

an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal

a functional unit; and

an activation circuit that activates the functional unit in response to the input signal from the speaker exceeding a threshold level, wherein the functional unit is coupled to the output circuit and begins an output operation to drive the speaker in response to being activated by the activation circuit.

5. The system of claim 4, wherein:

the functional unit comprises a memory array and access circuitry capable of reading values from the memory array; and

the output circuit comprises a converter coupled to the access circuitry, wherein the converter converts a series of values read by the access circuitry into an analog signal that determines the output signal.

6.(Amended) The system of claim 5, wherein the input circuit comprises:
an amplifier coupled to the first terminal;

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a second converter coupled to the amplifier and the access circuitry, wherein the second converter converts the input signal from the speaker into a series of values read that the access circuitry writes to the memory array.

7.(Amended) The system of claim 4, wherein the activation circuit includes a delay element coupled to prevent activation of the functional unit during a period following completion of an operation of the functional unit.

8.(Amended) A sound processing system comprising:

a speaker;

an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:

an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an output signal to drive the speaker;

an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal;

a memory array; and

access circuitry capable of reading values from the memory array,

wherein:

the output circuit comprises a converter coupled to the access circuitry, wherein the converter converts a series of values read by the access circuitry into an analog signal that determines the output signal.

9.(Amended) The system of claim 8, wherein the input circuit comprises:

an amplifier coupled to the first terminal;

a second converter coupled to the amplifier and the access circuitry, wherein the second converter converts the input signal from the speaker into a series of values read that the access circuitry writes to the memory array.

(Claim 10 has been cancelled.)

11.(Amended) A sound processing system comprising:

a speaker;

an integrated circuit having a first terminal coupled to the speaker, the integrated circuit further comprising:

an output circuit coupled to the first terminal, wherein the output circuit applies to the first terminal an output signal to drive the speaker; and

an input circuit coupled to the first terminal, wherein the input circuit processes an input signal from the speaker via the first terminal,

wherein the integrated circuit is in a three pin package including a first pin connected to the speaker and the first terminal of the integrated circuit, a second pin for connection to a power supply, and a third pin for connection to ground.

12. The system of claim 11, wherein the three pin package is a T092 package.

(Claims 13-16 have been cancelled.)

17.(Twice Amended) An integrated circuit comprising:

an input/output pin;

a sound processing circuit;

an output circuit coupled to the input/output pin, wherein the output circuit applies to the input/output pin an output signal representing a sound;

an activation circuit coupled to the input/output pin and the functional unit, wherein in response to an input signal from the input/output pin, the activation circuit activates the sound processing circuit;

an input circuit coupled to the input/output pin, wherein the input circuit, when active, transfers the input signal received from the input/output pin to the sound processing circuit; and

a control circuit coupled to the sound processing circuit, wherein the control circuit selects an operation performed by the processing circuit when the activation circuit activates the sound processing circuit, and

wherein the sound processing circuit comprises:

a first functional unit that performs an output operation to generate a signal to the output circuit and a second functional unit that performs an input operation to processes the input signal from the input circuit;

a memory array;

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a read circuit coupled to the memory array, wherein the read circuit is part of the first functional unit and the output operation includes reading from the memory array a series of values representing a sound; and

a write circuit coupled to the memory array, wherein the write circuit is part of the second functional unit and the input operation includes writing to the memory array a series of values representing the input signal.

18.(Twice Amended) The integrated circuit of claim 17, wherein the activation circuit comprises a delay element coupled to prevent the activation circuit from activating the sound processing circuit during a delay period following completion of an operation by the sound processing circuit.

19.(Amended) The integrated circuit of claim 17, further comprising a die and a three-pin package in which the die is mounted, the three-pin package having exactly three pins including the input/output, a pin for connection to a power supply, and a pin for connection to ground.

20. A method for operating a sound processing system, comprising:
connecting a terminal of a sound processing circuit to a speaker;
creating a vibration in the speaker that causes the speaker to generate an input signal to the terminal of the sound processing circuit;

activating a functional unit in the sound processing circuit in response to the input signal; and

in response to activating the functional unit, generating an output signal from the functional unit through the terminal to the speaker, wherein the output signal drives the speaker to produce a sound.

21. The method of claim 20, wherein creating the vibration comprises making a noise that causes a vibration in the speaker.

22. The method of claim 20, wherein creating the vibration comprises touching in the speaker.

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23. The method of claim 20, wherein the sound processing circuit is an integrated circuit and the terminal is a bi-direction input/output pin of the integrated circuit.

24. The method of claim 20, wherein generating the output signal comprises performing an output operation, and the method further comprising disabling activation of the functional unit during a delay time following the completion of the output operation.

25. The system of claim 6, wherein the output signal is derived from said series of values.

26. The system of claim 9, wherein the output signal is derived from said series of values.

27. The integrated circuit of claim 17, wherein the output signal is derived from said series of values.

28. The method of claim 20, further comprising:
recording an audio input by said functional unit through the speaker prior to creating the vibration, wherein the output signal is derived from the audio input.

29.(Amended) An integrated circuit comprising:
an input/output pin;
a memory array; and
a sound processing circuit including:
a write circuit coupled to the memory array and to the input/output pin, wherein the write circuit performs an input operation that includes writing to the memory array a series of values representing an audio signal received from the input/output pin; and
a read circuit coupled to the memory array and to the input/output pin, wherein the read circuit performs an output operation that includes reading from the memory array and supplying to the input/output pin a series of values representing said audio signal.

30. The integrated circuit of claim 29, wherein said memory array is comprised of non-volatile memory cells.

31. The integrated circuit of claim 29, wherein said series of values are analog values.

32. The integrated circuit of claim 30, wherein said memory array comprises a FLASH EEPROM memory.

33. The integrated circuit of claim 29, further comprising:
an activation circuit coupled to the input/output pin and to the sound processing circuit, wherein the sound processing circuit is activated by the activation circuit to supply said audio signal to the input/output pin in response to an input signal received from the input/output pin.

34. A method for operating a sound processing unit, comprising:
connecting a terminal of a sound processing circuit to a speaker;
recording by the sound processing circuit an audio input received through the speaker;
generating an input signal to the terminal of the sound processing circuit; and
in response to the input signal, supplying from the sound processing circuit through the terminal to the speaker an output signal derived from the audio input, wherein the output signal drives the speaker to produce a sound.

35. The method of claim 34, wherein said input signal is generated by creating a vibration in the speaker.

36. The method of claim 34, wherein the sound processing circuit is an integrated circuit and the terminal is a bi-directional input/output pin of the integrated circuit.